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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,436	12/12/2001	Timothy B. Cowles	00-0058.02	4282

7590 02/07/2007

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EXAMINER	
TU, CHRISTINE TRINH LE	
ART UNIT	PAPER NUMBER
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/022,436	COWLES ET AL.	
	Examiner	Art Unit	
	Christine T. Tu	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *November 14, 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 64-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 64-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *Sep. 19, 2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Double Patenting

2. Claims 1 and 64-65 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,918,072. Although the conflicting claims are not identical, they are not patentably distinct from each other because the patent substantially teaches the claimed invention. The patent does not explicitly disclose the feature of testing the memory die. Patent '072, however, teaches the feature of checking a group of memory cells on said memory chip for a defect (column 16 lines 34-35). It is be obvious for a person of ordinary skill in the art at the time the invention was made to realize that the checking feature (for checking a group of memory cells on a memory chip for a defect) of Patent '072 would have been a process of testing a memory die. One having ordinary skill in the art would be motivated to realize so because in order to test a memory die/chip, memory cells on the die/chip would have been checked to determine whether any defective(s) on any memory cell.

3. Claims 1 and 64-65 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 56 of U.S. Patent No. 6,918,072. Although the conflicting claims are not identical, they are not patentably distinct from each other because the patent substantially teaches the claimed invention. The patent does not explicitly disclose the feature of testing the memory die. Patent '072, however, teaches the feature of identifying a defective memory cell on the chip (column 21 lines

24-25). It is be obvious for a person of ordinary skill in the art at the time the invention was made to realize that the identifying feature (for identifying a defective memory cell) of Patent '072 would have been a process of testing a memory die. One having ordinary skill in the art would be motivated to realize so because in order to test a memory die/chip, each memory cell on the die/chip would have been checked to identify/determine whether any defective(s) on that memory cell.

Claim Rejections - 35 USC § 101 and 112, 1st ¶

4. Claims 1, 64 and 65 are rejected under 35 U.S.C. 101 because the claimed invention is not supported by either a specific and substantial asserted utility or a well established utility.

Claims 1, 64, and 65 are amended with the limitation of "... wherein said storing replaces any previously stored address or partial address". Such limitation is not support by the specification nor drawings.

In the specification, page18, lines 3-4 of ¶ [0067], the specification states that "redundant column address stored in redundancy register 71". In addition, on page 21, lines 17-18 of ¶ [0074], the specification also states that "redundant column address ... may be stored in redundant register 71". In other words, the specification shows the redundancy register (71) only stores the redundant column address. However, The specification does not show that such a storing feature (of the redundancy register [71])

comprises a feature of replacing any previous stored address or partial address within the redundancy register (71).

Moreover, none of the drawings shows a storing feature that comprises any previously stored address or partial address.

Claims 1, 64, 65 are also rejected under 35 U.S.C. 112, first paragraph. Specifically, since the claimed invention is not supported by either a specific and substantial asserted utility or a well established utility for the reasons set forth above, one skilled in the art clearly would not know how to use the claimed invention.

Claim Objections

5. Claims 66 and 67 are objected to because of the following informalities:

Claims 66 and 67:

At line 2, the word "cell" should be replaced with "cells". This is because a row or a column should comprise two or more cells

Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. Claims 1-6 and 64-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brauch (6,550,023).

Claim 1:

Brauch discloses the invention substantially as claimed. Brauch teaches (figure 1) that a chip (2) comprises a memory (4), a BIST functional block (6) and bitmap storage (18). The BIST functional block (6) is firmware that controls the execution of on-chip memory tests to detect and locate defects in the memory (4). When a corrupt cell is detected, the bitmap storage (18) stores comparison mismatch information comprising a complete bitmap of the precise location of failed cells in the memory (4) (figure 1, column 3 lines 15-48).

Brauch does not explicitly teach that the testing and storing acts are performed outside of a production facility of a die. It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that Brauch's BIST's on-chip memory testing and storing would have been performed outside of a production/manufacturing facility of a die. One having ordinary skill in the art would be motivated to realize so because Brauch teaches that the BIST's on-chip memory testing and storing is performed upon power up and in real-time (column 1 lines 43-60, column 5 line 62-column 6 line 8).

Claims 2, and 4-6

Brauch does not explicitly teach that the die is part of an electronic system, a computer system or a processing system. Brauch teaches that a test of an on-chip cache is done when turning on a combination of a microprocessor and its on-chip cache (column 6 lines 16-20). It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that Brauch's chip/IC (2) would have been a part of an electronic system, a computer system or a processing system. One having ordinary skill in the art would be motivated to realize so because Brauch's chip/IC is part of the combination (of the microprocessor and its on-chip cache) (as taught by Brauch [column 6 line 19]).

Claim 3:

Brauch's memory test is perform upon the power is up (column 1 lines 43-60).

Claim 64:

Brauch discloses the invention substantially as claimed. Brauch teaches (figure 1) that a chip (2) comprises a memory (4), a BIST functional block (6) and bitmap storage (18). The BIST functional block (6) is firmware that controls the execution of on-chip memory tests to detect and locate defects in the memory (4). When a corrupt cell is detected, the bitmap storage (18) stores comparison mismatch information comprising a complete bitmap of the precise location of failed cells in the memory (4) (figure 1, column 3 lines 15-48).

Brauch does not explicitly teach that the testing and storing acts are performed in a field. It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that BIST's on-chip memory testing and storing (taught by Brauch) would have been performed in real time. One having ordinary skill in the art would be motivated to realize so because that recited "the field" is not explicitly recited with any particular field or environment.

Claim 65:

Brauch discloses the invention substantially as claimed. Brauch teaches (figure 1) that a chip/IC (2) comprises a memory (4), a BIST functional block (6) and bitmap storage (18). The BIST functional block (6) is firmware that controls the execution of on-chip memory tests to detect and locate defects in the memory (4). When a corrupt cell is detected, the bitmap storage (18) stores comparison mismatch information comprising a complete bitmap of the precise location of failed cells in the memory (4) (figure 1, column 3 lines 15-48).

Brauch does not explicitly teach that the die is part of a processing system. Brauch teaches that a test of an on-chip cache is done when turning on a combination of a microprocessor and its on-chip cache (column 6 lines 16-20). It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that Brauch's chip/IC (2) would have been a part of a processing system. One having ordinary skill in the art would be motivated to realize so because Brauch's chip/IC is part of the combination (of the microprocessor and its on-chip cache) (as taught by Brauch [column 6 line 19]).

7. Claims 66-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brauch (6,550,023) in view of Patti (6,236,602).

Claims 66-67:

Brauch does not explicitly teach storing feature for storing a column or a row address of the defective memory cells. Patti, however, teaches CAMs (42 and 43). The CAM (42) stores bad column address and CAM (43) stores a bad row address (figure 1).

It would have been obvious to one skilled in the art at the time the invention was made to realize that Brauch's bitmap storage (18) would have comprised of Patti's CAMs (42 & 43). One having ordinary skill in the art would be motivated to realize so because Brauch teaches that the address of a mismatching bit(s) of that corrupted cells of the address word is stored into the bitmap storage (18) (figure 1, column 3 lines 35-44 and column 4 lines 64-65).

Response to Arguments

8. Applicant's arguments with respect to claims 1, 64 and 65 have been considered but are moot in view of the new ground(s) of rejection.

For nonstatutory obviousness-type double patenting rejection, applicant did not immediately address such rejection. Therefore, such rejection is rejected again as in the previously office action (see rejection on ¶s 2 and 3 above).

For claims 1, 64 and 65, applicants argue that Wada does not teach or suggest the amended limitation of the storing feature comprises replacing any previously stored

address or partial address. However, such an amended limitation is not supported by the specification or drawings (see rejection on ¶4 above).

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (571)272-3831. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571)272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christine T. Tu
Primary Examiner
Art Unit 2138

February 2, 2007